EAST Browser - L16: (20) scan near2 c... | JP 01157180 A | Tag: S.T1 | Doc: 3/20 (SORTED) | Format : FULL

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DERWENT-ACC-NO: 1989-217931

DERWENT-WEEK: 198930



TITLE: Interlacing-to-non-interlacing display scan converter - writes interlacing image into empty memory area each time one-raster image is read out from frame memory NoAbstract Dwg 1,3/3

PATENT-ASSIGNEE: EASEL KK[EASEN]

PRIORITY-DATA: 1987JP-0315742 (December 14, 1987)

PATENT-FAMILY:

| PUB-NO | PUB-DATE | LANGUAGE | PAGES | MAIN-IPC |
|---|---|---|---|---|
| JP 01157180 A | June 20, 1989 | N/A | 008 | N/A |

APPLICATION-DATA:

| PUB-NO | APPL-DESCRIPTOR | APPL-NO | APPL-DATE |
|---|---|---|---|
| JP 01157180A | N/A | 1987JP-0315742 | December 14, 1987 |

Details | Text | Image | HTML | FULL

| | U | 1 | Document ID | Issue Date | |
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| 3 | ☐ | ☑ | JP 01157180 A | 19890620 | Interlacin interlacin image is r |
| 4 | | | JP 03268737 A | 19911129 | LIVING B |

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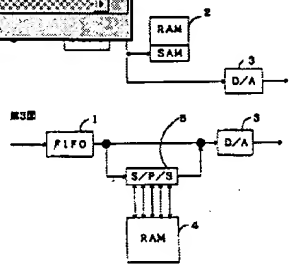
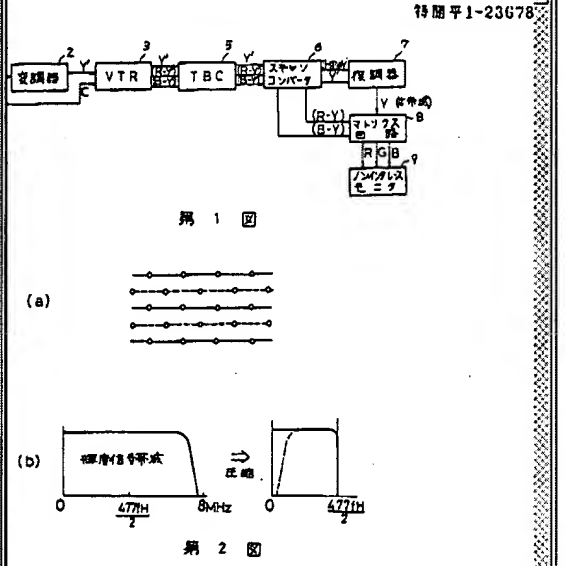



signal of one horizontal scanning period before to restore the wide band luminance signal.

CONSTITUTION: A wide band luminance signal Y and a color signal C separated from a color video signal are inputted to an input terminal 1, and the signal Y has the band compressed to about 1/2 by dot interlacing of a modulator 2. A compressed luminance signal Y' and the color signal C are recorded on a VTR 3, and jitter is removed by a time base corrector 5 to obtain the luminance signal Y' and a color difference signal R-Y', and a scan converter 6 is used to generate the luminance signal Y' and the luminance signal Y' of one line before based on these signals, and they are supplied to a demodulator 7. Simultaneously, the output of the converter 6 is inputted to a matrix circuit 8, and this output and the output of the demodulator 7 are converted to R, G, and B signals, and they are displayed on a non-interlace monitor 9.





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第 2 図

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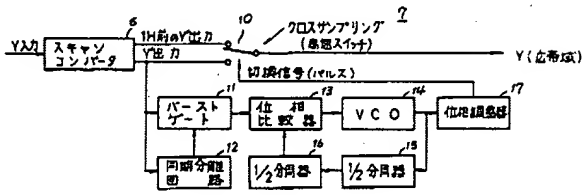


第 5 図

# PATENT ABSTRACTS OF JAPAN

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(71)Applicant : IIZERU:KK

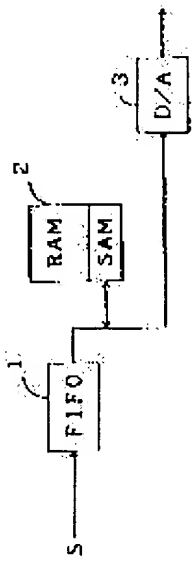
(72)Inventor : KUMAGAI RYOHEI

## (54) SCAN CONVERTER

(57)Abstract:

PURPOSE: To decrease memory capacity by writing a next interlace image to a frame memory part, to which a reading is complete, or moving a raster in a line memory part to the frame memory part to which the reading is executed.

CONSTITUTION: The frame memory part, which can hold the interlace image equivalent to one picture, and the line memory part, which can hold an image for one raster part, are allocated to the RAM part of a dual port memory 2. The control of the dual port memory 2 is executed by an address reading and writing control means. Then, each time one raster part is read from the frame memory part, the next interlace image is written per raster to a memory area, in which the reading is completed, or, after the next interlace image is written per raster to the line memory part, the image equivalent to one raster is read from the frame memory part and the raster in the line memory part is moved to a storing area in which the reading is executed.

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